DECLARATION

I, Keita NOGUCHI, a national of Japan, c/o Central Research Laboratory of Hitachi, Ltd. of 1-280, Higashikoigakubo, Kokubunji-shi, Tokyo, Japan, do hereby solemnly and sincerely declare:

1) THAT I am well acquainted with the Japanese language and English language, and
2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No.1994-316444 filed on December 20, 1994.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true ; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 14th day of March , 2005

Keita NOGUCHI

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[Name of Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE

[Claims]

[Claim 1] A semiconductor device in which a semiconductor pellet is mounted on a pellet mounting area of a main surface of a base substrate, and first electrode pads mounted on a rear surface of the base substrate are electrically connected to external terminals arranged on the main surface of the semiconductor pellet,

wherein the semiconductor pellet is mounted on the pellet mounting area of the main surface of the base substrate with its main surface downward, second electrode pads electrically connected to the first electrode pads are arranged on the rear surface of the base substrate, and the external terminals of the semiconductor pellet and the second electrode pads of the base substrate are electrically interconnected through bonding wires passing through slits formed in the base substrate.

[Claim 2] A semiconductor device according to claim 1, wherein the slits are formed along the directions of rows of a plurality of the external terminals that are arranged on the main surface of the semiconductor pellet, and the slits are located on the external terminals of the semiconductor pellet.

[Claim 3] A semiconductor device according to claims 1

or 2, wherein the second electrode pads of the base substrate, are mounted in both areas of the rear surface on the base substrate divided by the slits.

[Claim 4] A semiconductor device according to claim 3, wherein a power supply is supplied to the second electrode pads arranged on one of both areas of the rear surface on the base substrate divided by the slits, and a signal is applied to the second electrode pads arranged on the other of both areas of the rear surface of the base substrate divided by the slits.

[Claim 5] A semiconductor device according to any one of claims 1 to 4, wherein the rear surface of the semiconductor pellet is exposed from a resin sealing body which covers the peripheral area of the main surface of the base substrate.

[Claim 6] A semiconductor device according to any one of claims 1 to 5, wherein the bonding wires are sealed with the resin sealing body.

[Claim 7] A semiconductor device according to any one of claims 1 to 6, wherein bump electrodes are formed on the surfaces of the first electrode pads on the base substrate.

[Detailed description of the Invention]

[0001]

[Technical Field]

The present invention relates to a semiconductor device and more particularly to a technology effectively applied to a semiconductor device, the device having a structure in which a semiconductor pellet is mounted on a pellet mounting area on the main surface of a base substrate and in which electrode pads on the back of the base substrate are electrically connected to external terminals on the main surface of the semiconductor pellet.

[0002]

[Background Art]

A semiconductor device with a ball grid array (BGA) structure has been introduced as a semiconductor device having a high level of integration. The semiconductor device employing the BGA structure, as shown in FIG. 10 (cross section of an essential part), has a semiconductor pellet 2 mounted on a pellet mounting area of the main surface of the base substrate 1 and a plurality of bump electrodes 4 arranged in grid on the back of the base substrate 1 opposite the main surface.

[0003]

The base substrate 1 may be made from for example a printed wiring board of two-layer wiring structure. A

plurality of electrode pads 1A are arranged in a peripheral area of the main surface of the base substrate 1 (around the pellet mounting area), while a plurality of electrode pads 1B are arranged on the back of the base substrate 1 opposite the main surface. The electrode pads 1A are electrically connected to through-hole conductors 1C via conductors $1A_1$ arranged on the main surface of the base substrate 1. The electrode pads 1B are electrically connected to the through-hole conductors 1C via conductors $1B_1$ arranged on the back of the base substrate 1. On the electrode pads 1B the bump electrodes 4 are electrically and mechanically connected.

[0004]

The semiconductor pellet 2, for example, may comprise mainly a semiconductor substrate 2B of single-crystal silicon. On the main surface of the semiconductor substrate 2B (device forming surface) is formed a logic circuit system, a memory circuit system or a combination of these systems. A plurality of external terminals (bonding pads) 2A are arranged on the main surface of the semiconductor substrate 2B. The external terminals 2A are formed in the top of the interconnect layers formed on the main surface of the semiconductor substrate 2B.

[0005]

The external terminals 2A on the semiconductor

pellet 2 are electrically connected to the electrode pads 1A on the main surface of the base substrate 1 through bonding wires 6. In other words, the external terminals 2A on the semiconductor pellet 2 are electrically connected to the electrode pads 1B through the bonding wires 3, electrode pads 1A, conductors $1A_1$, through-hole conductors 1C and conductors $1B_1$.

[0006]

The semiconductor pellet 29 the bonding wires 6,, etc. are sealed with a resin sealing body 7 formed on the main surface of the base substrate 1.

[0007]

The semiconductor device having such a configuration is mounted on a mounting surface of a mounting board. The bump electrodes 4 of the semiconductor device are electrically and mechanically connected to the electrode pads arranged on the mounting surface of the mounting board.

[0008]

The semiconductor device of such a BGA structure is disclosed, for example, in the Nikkei Electronics (Feb. 28, 1994, pp. 111-117) published by Nikkei McGraw-Hill.

[0009]

[Problems to be Solved by the Invention]

In the semiconductor device, the electrode pads 1A

arranged on the main surface of the base substrate 1 are electrically connected through the through-hole conductors 1C to the electrode pads 1B arranged on the back of the base substrate 1. The through-hole conductors 1C comprises a hole area formed within a through-hole in the base substrate 1 and a land area (fringe portion) formed on the main surface and back surface of the base substrate 1. The inner diameter of the through-hole may be around ϕ 0.3 mm and the outer diameter of the land area of the through-hole conductor 1C may be about ϕ 0.6 mm. The inner diameter of the through-hole and the outer diameter of the land area of the through-hole conductor 1C are set large compared to the widths of the conductors $1A_1$ (or conductors $1B_1$) electrically connecting the electrode pads 1A (or electrode pads 1B) and the through-hole conductors 1C.

[0010]

The circuit systems formed on the semiconductor pellets 2 have tended to grow in their level of integration. With enhanced integration of the circuit system, the number of external terminals 1A of the semiconductor pellet 2 and the number of electrode pads 1A of the base substrate 1 increase. That is, the number of through-hole conductors 1C electrically connecting the electrode pads 1A and the electrode pads 1B increases as

the integration of the circuit system are enhanced. Hence, there has been a problem that the external size of the base substrate 1 increases by a number corresponding to the number of the through-hole conductors 1C, which in turn increases the size of the semiconductor device as a whole.

[0011]

As the number of the through-hole conductors 1C increases, they are positioned outwardly away from the semiconductor pellet 2. This inevitably extends the length of the conductors $1A_1$ (or the conductors $1B_1$) electrically connecting the electrode pads 1A (or the electrode pads 1B) and the through-hole conductors 1C. This, in turn, increases inductance and reduces the operating speed of the semiconductor device.

[0012]

An object of this invention is to provide a technology that allows a reduction in the size of the semiconductor device.

[0013]

Another object of this invention is to provide a technology that allows an increase in the operating speed of the semiconductor device.

[0014]

These and other objects and novel features of this

invention will become apparent from the following description of this specification and the accompanying drawings.

[0015]

[Means for Solving the Problems]

Representative aspects of this invention may be briefly summarized as follows.

[0016]

In a semiconductor device in which a semiconductor pellet is mounted on a pellet mounting area of the main surface of a base substrate, and first electrode pads mounted on the rear surface of the base substrate are electrically connected to external terminals arranged on the main surface of the semiconductor pellet,

the semiconductor pellet is mounted on the pellet mounting area of the main surface of the base substrate with its main surface downward, a second electrode pads electrically connected to the first electrode pads are arranged on the rear surface of the base substrate, and the external terminals of the semiconductor pellet and the second electrode pads of the base substrate are electrically interconnected through bonding wires passing through slits formed in the base substrate.

[0017]

[Operation]

According to the above means, the external terminals of the semiconductor pellet and the first electrode pads of the base substrate can be electrically connected through the bonding wires and the second electrode pads, so it is possible to eliminate the through-hole conductors used to electrically connect the electrode pads arranged in the periphery of the main surface of the base substrate and the first electrode pads arranged on the back surface of the base substrate in prior structures. This allows the external size of the base substrate to be reduced by an amount corresponding to an area occupied by the through hole conductors (land area), thus reducing the size of the semiconductor device as a whole.

[0018]

Further, because the first electrode pads can be put closer to the second electrode pads by an amount corresponding to an area occupied by the through hole conductors, the conductors of the base substrate that electrically connect the second electrode pads and the first electrode pads can be reduced in length. As a result, inductance can be reduced and the operating speed of the semiconductor device increased.

[0019]

[Embodiments]

The construction of this invention is described in

the following in conjunction with embodiments that apply this invention to a semiconductor device using the BGA structure.

[0020]

In the drawings used for explaining the embodiments, components with identical functions are given like reference numerals and their explanations are not repeated.

[0021]

(Embodiment 1)

The outline construction of a semiconductor device, as a first embodiment of this invention, that uses the BGA structure is shown in FIG. 1 (plan view of the main surface side), FIG. 2 (cross section taken along the line A-A of FIG. 1), FIG. 3 (enlarged cross section of an essential part of FIG. 2) and FIG. 4 (enlarged plan view showing the back side of an essential part of the semiconductor device with the resin sealing body removed).

[0022]

As shown in FIGS. 1, 2, 3 and 4, the semiconductor device has a semiconductor pellet 2 mounted on a pellet mounting area of the main surface of a base substrate 1, with a plurality of bump electrodes 4 arranged in grid on the back of the base substrate 1 opposite the main surface.

[0023]

The base substrate 1 may be formed of a two-layer

printed circuit board. On the back of the base substrate 1 are formed a plurality of electrode pads 1A and electrode pads 1B, which are electrically interconnected through conductors $1B_1$ on the back of the base substrate 1.

[0024]

On the surfaces of the electrode pads 1B are formed bump electrodes 4 that are electrically and mechanically connected to them. The bump electrodes 4 may be formed of, for instance, a Pb-Sn alloy.

[0025]

The semiconductor pellet 2 is mounted, with its main surface (underside in FIGS. 2 and 3) downward, on the pellet mounting area of the main surface of the base substrate 1. That is, the semiconductor pellet 2 is mounted facedown on the pellet mounting area of the main surface of the base substrate 1. Interposed between the main surface of the semiconductor pellet 2 and the pellet mounting area of the main surface of the base substrate 1 is an insulating layer 3, which may be formed of a polyimide-, epoxy- or silicon-base resin or the like.

[0026]

The semiconductor pellet 2 may be rectangular on a plane surface and may mainly be comprised of a semiconductor substrate 1B made of single-crystal silicon. On the main surface (device forming surface) of the

semiconductor substrate 1B are formed a logic circuit system, a memory circuit system or a combination of these systems. Also on the main surface of the semiconductor substrate 1B, a plurality of external terminals 2A (bonding pads) are arranged along the sides of the rectangular surface. The external terminals 2A are formed on the top of interconnect layers on the main surface of the semiconductor substrate 2B. That is, the external terminals 2A are arranged in the periphery of the main surface of the semiconductor pellet 2 along each of the sides.

[0027]

The external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1 are electrically interconnected through bonding wires 6 running in slits 5 formed in the base substrate 1. The bonding wires 6 may be of gold (AU), copper (Cu) or aluminum (Al), and may be formed by coating a surface of a metal wire with insulating resin or the like. The bonding wires 6 may be connected by a bonding method that utilizes ultrasonic vibrations in combination with thermo-compression.

[0028]

The slits 5 in the base substrate 1 are formed in the directions of the rows of the external terminals 2A

that are arranged along each side of the main surface of the semiconductor pellet 2. That is, the base substrate 1 of this embodiment has four slits 5, each of which is located above the external terminals 2A of the semiconductor pellet 2.

[0029]

The electrode pads 1A of the base substrate 1 are placed in both areas of the back of the base substrate 1 divided by the slits 5. The electrode pads 1A located in one of the areas of the back of the base substrate 1 demarcated by the slits 5 (inside the semiconductor pellet 2) are supplied with a power supply such as an operation voltage (3.3 V for instance) and a reference voltage (0 V for instance). The electrode pads 1A located in the other area of the back of the base substrate 1 demarcated by the slits 5 (outside the semiconductor pellet 2) receive a signal such as an input/output signal and a control signal.

[0030]

The semiconductor pellet 2 is provided with 100 external terminals 2A on each side at a pitch of about 100 μm, for example. The number of external terminals 2A is increased as the level of integration and the operating speed of the circuit system mounted on the semiconductor pellet 2 increase.

[0031]

The one area of the back of the base substrate 1 demarcated by the slits 5 is provided with, for example, 50 electrode pads 1A for each side of the semiconductor pellet 2; and the other area is provided with, for instance, 50 electrode pads 1A for each side of the semiconductor pellet 2. Because the electrode pads 1A cannot be made as small as the external terminals 2A of the semiconductor pellet 2, the pitch of the electrode pads 1A is set wider than that of the external terminals 2A, for instance, at around 200 μm. That is, because the electrode pads 1A of the base substrate 1 are arranged in two rows for each side of the semiconductor pellet 2, the length of the electrode pads 1A corresponding to one side of the semiconductor pellet 2 can be made almost equal to that of the external terminals 2A arranged along one side of the semiconductor pellet 2 even if the pitch of the electrode pads 1A of the base substrate 1 is set to two times that of the external terminals 2A of the semiconductor pellet 2. Furthermore, the electrode pads 1A of the base substrate 1 can be located at positions facing the corresponding external terminals 2A of the semiconductor pellet 2.

[0032]

The peripheral area of the main surface of the base substrate 1 excluding the pellet mounting area is covered

with a resin sealing body 7, which seals the bonding wires 6. That is, the resin sealing body 7 is formed on the main surface side and the back surface side of the base substrate 1. The resin sealing body 7 is formed by, for example, the transfer molding method. The resin sealing body 7 is made from epoxy resin 7A containing an epoxy-base phenol hardened resin, silicone rubber and filler for reducing stresses. The resin sealing body 7 may be formed by the potting method, and as shown in FIG. 5 (cross section), on the back of the base substrate 1 excluding each area of the electrode pads 1A and the electrode pads 1B.

[0033]

The back of the base substrate 1 facing the main surface of the semiconductor pellet 2 is exposed from the resin sealing body 7 that covers the peripheral area of the base substrate 1.

[0034]

The semiconductor having such a structure is mounted on a mounting surface of a mounting board, with the bump electrodes 4 of the semiconductor device electrically and mechanically connected to electrode pads arranged on the mounting surface of the mounting board.

[0035]

This embodiment offers the following advantages.

[0036]

(1) In a semiconductor device having the BGA structure in which a semiconductor pellet 2 is mounted on a pellet mounting area of the main surface of a base substrate 1, and electrode pads (a first electrode pads) 1B mounted on the rear surface of the base substrate 1 are electrically connected to external terminals 2A arranged on the main surface of the semiconductor pellet 2, the semiconductor pellet 2 is mounted on the pellet mounting area of the main surface of the base substrate 1 with its main surface downward, electrode pads(second electrode pads) 1A electrically connected to the electrode pads 1B are arranged on the rear surface of the base substrate 1, and the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1 are electrically interconnected through bonding wires 6 passing through slits 5 formed in the base substrate 1. Because with this construction the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1B of the base substrate 1 can be electrically interconnected through the bonding wires 6 and electrode pads 1A, it is possible to eliminate the through hole conductors 1C used to electrically connect the electrode pads 1A formed on the periphery of the base substrate 1 and the electrode pads 1B formed on the back surface of the base substrate.

This in turn allows the base substrate 1 to be reduced in size by an amount corresponding to the occupied area of the through hole conductors (area of land region), which contributes to size reduction of the semiconductor device.

[0037]

Because the electrode pads 1B can be put closer to the electrode pads 1A by a distance corresponding to the occupied area of the through hole conductors, it is possible to shorten the length of the conductors $1B_1$ of the base substrate 1 that electrically connect the electrode pads 1A with the electrode pads 1B. This reduces signal paths between the electrode pads 1A and the electrode pads 1B, which results in reduction of the inductance, thereby increasing the operation speed of the semiconductor device.

[0038]

(2) The slits 5 extends in the directions of rows of a plurality of external terminals 2A arranged on the main surface of the semiconductor pellet 2 and are located at positions over the external terminals 2A. With this construction, the slits 5 are arranged within the area occupied by the semiconductor pellet 2, so that the increase in size of the base substrate 1 corresponding to the area occupied by the slits 5 can be suppressed.

[0039]

(3) The electrode pads 1A are arranged in two opposite areas of the back of the base substrate 1 divided by the slits 5. This construction allows an increase in the number of power supply paths for electrically connecting the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1. This in turn makes it possible to reduce power supply noise generated at time of simultaneous switching of signals, thereby preventing malfunctions of the semiconductor device.

[0040]

Further, even when the pitch of the electrode pads 1A of the base substrate 1 is set larger than that of the external terminals 2A of the semiconductor pellet 2, the length of the row of the electrode pads 1A for each side of the semiconductor pellet 2 can be made almost equal to the length of the row of the external terminals 2A for each side of the semiconductor pellet 2. This prevents an increase in the length of the bonding wires 6, which is dependent on the length of the row of the electrode pads 1A. As a result, it is possible to prevent the bonding wires 6 from being deformed by the flow of resin when the bonding wires 6 are sealed by the resin sealing body 7 according to the transfer molding.

[0041]

Further, because the electrode pads 1A can be located at positions on the base substrate 1 facing the external terminals 2A of the semiconductor pellet 2, the lengths of the bonding wires 6 can be made uniform, which in turn makes uniform the inductances of the signal paths between the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1.

[0042]

(4) The back of the semiconductor pellet 2 opposing its main surface is exposed from the resin sealing body 7 that covers the peripheral area around the main surface of the base substrate 1. This structure allows the heat generated by the operation of the circuit system mounted on the semiconductor pellet 2 to be released from the back of the semiconductor pellet 2 to outside, thus enhancing the heat dissipation efficiency of the semiconductor device.

[0043]

(5) The bonding wires 6 are sealed with the resin sealing body 7. This structure prevents the bonding wires 6 from being deformed due to external impacts and contacts, thus enhancing the electric reliability of the semiconductor device.

[0044]

(6) The resin sealing body 7 is formed both on the

main surface side and the back surface side of the base substrate 1. This structure prevents the resin sealing body 7 from becoming separated from the base substrate 1 due to the thermal stresses generated during a temperature cycle test or when the bump electrodes 4 are connected. This in turn enhances the reliability of the semiconductor device.

[0045]

(Embodiment 2)

The outline configuration of a semiconductor device as the second embodiment of this invention that employs a BGA structure is shown FIG. 6 (cross section) and FIG. 7 (an enlarged plan view showing the back side of an essential part of the semiconductor device with the resin sealing body removed).

[0046]

As shown in FIGS. 6 and 7, the semiconductor device has the semiconductor pellet 2 mounted with a facedown system on the pellet mounting area of the main surface of the base substrate 1 with an insulating layer 3 disposed therebetween. A plurality of bump electrodes 4 are arranged in grid on the back of the base substrate 1.

[0047]

Arranged in the central area of the main surface of the semiconductor pellet 2 is a plurality of external

terminals 2A along the longer sides thereof, which are electrically connected to the electrode pads 1A arranged on the back of the base substrate 1 through the bonding wires 6 passing through the slits 5 formed in the base substrate 1. A plurality of electrode pads 1A are electrically connected to the corresponding electrode pads 1B arranged on the back of the base substrate 1 through conductors $1B_1$. Bump electrodes 4 are electrically and mechanically connected to the surfaces of the electrode pads 1B. That is, the external terminals 2A of the semiconductor pellet 2 are electrically connected to the electrode pads 1B through the bonding wires 6, electrode pads 1A and conductors $1B_1$.

[0048]

The slits 5 of the base substrate 1 are formed in the central area of the main surface of the semiconductor pellet 2 along the direction of the row of the external terminals 2A arranged along the longer side of the semiconductor pellet 2. The slits 5 are tapered so that its opening on the back side of the base substrate 1 is greater than the opening on the main surface side.

[0049]

As described above, this embodiment offers similar effects and advantages to those of the first embodiment. With the slits 5 tapered, it is possible to prevent

contact between the base substrate 1 and a bonding tool when one end of the bonding wires 6 is bonded to the external terminals 2A of the semiconductor pellet 2. This in turn raises the yield of semiconductor device assembly in the bonding process.

[0050]

(Embodiment 3)

The outline configuration of a semiconductor device as the third embodiment of this invention that employs a BGA structure is shown in FIG. 8 (a plan view of an essential part of the back side showing the state of the back side on which the resin sealing body is removed).

[0051]

As shown in FIG. 8, the semiconductor device has a semiconductor pellet 2 mounted with a facedown system on a pellet mounting area of the main surface of the base substrate 1, with an insulating layer 3 disposed therebetween. Bump electrodes 4 are arranged in grid on the back of the base substrate 1.

[0052]

At the outer periphery of the main surface of the semiconductor pellet 2, a plurality of external terminals 2A are arranged along the sides of the pellet. At the central portion of the main surface of the semiconductor pellet 2, a plurality of external terminals 2A are

arranged along the longer or shorter side of the pellet. The external terminals 2A are electrically connected to the electrode pads 1A arranged on the back of the base substrate 1 by bonding wires 6 passing through slits 5 formed in the base substrate 1. The electrode pads 1A are electrically connected to electrode pads 1B arranged on the back of the base substrate 1 through conductors $1B_1$. Bump electrodes 4 are electrically and mechanically connected to the surfaces of the individual electrode pads 1B. That is, the external terminals 2A of the semiconductor pellet 2 are electrically connected to the electrode pads 1B through the bonding wires 6, electrode pads 1A and conductors $1B_1$.

[0053]

The slits 5 of the base substrate 1 are arranged at each sides of the semiconductor pellet 2 and also at the central portion of the semiconductor pellet 2. That is, the base substrate 1 of this embodiment has five slits 5, each of which is located above the external terminals 2A of the semiconductor pellet 2.

[0054]

As explained above, this embodiment offers the similar effects and advantages to those of the first embodiment. Because the slits 5 are arranged at the sides and the central portion of the semiconductor pellet 2, it

is possible to increase the number of external terminals 2A arranged on the main surface of the semiconductor pellet 2 and the number of electrode pads 1A arranged on the back of the base substrate 1. This allows an increase in the number of power supply paths for electrically connecting the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1. This in turn allows a further reduction in power supply noise generated when output signals are switched simultaneously. Furthermore, this construction makes it possible to increase the number of signal paths electrically connecting the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1 and therefore reduce the external size of the semiconductor pellet 2 limited by the number of external terminals 2A.

[0055]

Although this embodiment has been shown to have only one slit 5 formed at the central portion of the semiconductor pellet 2, slits 5 may be arranged parallel or crosswise to each other at the central part of the semiconductor pellet 2. By increasing the number of slits 5 in this way, it is possible to further increase the number of the electrode pads 1A of the base substrate 1 and the number of the external terminals 2A of the

semiconductor pellet 2.

[0056]

(Embodiment 4)

The outline configuration of a semiconductor device as the third embodiment of this invention that employs a BGA structure is shown in FIG. 9 (plan view of an essential part of the back side showing the state of the back side in which the resin sealing body is removed).

[0057]

As shown in FIG. 9, the semiconductor device has a semiconductor pellet 2 mounted facedown on a pellet mounting area of the main surface of the base substrate 1, with an insulating layer 3 disposed therebetween. Bump electrodes 4 are arranged in grid on the back of the base substrate 1. The base substrate 1 is formed of a printed circuit board of, for example, 3-layer wiring structure.

[0058]

At the outer periphery of the main surface of the semiconductor pellet 2, a plurality of external terminals 2A are arranged along the sides of the pellet. Each of the external terminals 2A are electrically connected to each of the corresponding electrode pads 1A arranged on the back of the base substrate 1 through bonding wires 6 passing through slits 5 formed in the base substrate 1.

[0059]

Of the electrode pads 1A, electrode pads $1A_2$ are formed integral with electrode plates 8A. The electrode plates 8A are electrically connected to other electrode plates 8A via through hole conductors (not shown) and internal wiring (not shown) in the base substrate 1. A reference voltage (0 V for example) as a power supply is supplied to the electrode plates 8A. Of the electrode pads 1A, electrode pads $1A_3$ are formed integral with an electrode plate 8B. An operating voltage (3.3 V for instance) as a power supply is applied to this electrode plate 8A.

[0060]

With this embodiment, because the through hole conductors 1C that electrically connect the electrode pads 1A on the main surface of the base substrate 1 and the electrode pads 1B on the back are eliminated, the electrode plates 8A and the electrode plate 8B can be arranged on the back of the base substrate 1. This allows the bump electrodes 4 to be freely located and shortens the distance between the external terminals 2A of the semiconductor pellet 2 and the pump electrodes 4. As a result, the inductance can be reduced, thereby increasing the operating speeds of the semiconductor device.

[0061]

The invention has been described in detail in

connection with representative embodiments of the invention. It is noted, however, that the invention is not limited to these embodiments but that many modifications may be made without departing from the spirit of the invention.

[0062]

It is possible for the present invention, for example, to be applied in a semiconductor device which has 3-layer wiring structure or more than 3-layer wiring structure.

[0063]

[Effects of the Invention]

Representative advantages disclosed by this application of this invention may be summarized as follows.

[0064]

It is possible to reduce the size of a semiconductor device in which the semiconductor pellet is mounted on the pellet mounting area of the main surface of the base substrate and in which the electrode pads arranged on the back of the base substrate are electrically connected to the external terminals arranged on the main surface of the semiconductor pellet.

[0065]

It is possible to increase the operating speed of the semiconductor device.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 is a plan view of the main surface side of the semiconductor device which employs the BGA structure being Embodiment 1 of the present invention.

[FIG. 2]

FIG. 2 is a cross section taken along the line A-A of FIG. 1.

[FIG. 3]

FIG. 3 is an enlarged cross section of an essential part of FIG. 2.

[FIG. 4]

FIG. 4 is an enlarged plan view showing the back side of an essential part of the semiconductor device with the resin sealing body removed.

[FIG. 5]

FIG. 5 is a cross section showing a modification of the semiconductor device.

[FIG. 6]

FIG. 6 is a cross section of the semiconductor device which employs a BGA structure being Embodiment 2 of the present invention.

[FIG. 7]

FIG. 7 is an enlarged plan view of an essential part of the back side showing the state of the back side of the

semiconductor device with the resin sealing body removed.

[FIG. 8]

FIG. 8 is a plan view of an essential part of the back side showing the state of the back side with the resin sealing body removed in the semiconductor device which employs a BGA structure being Embodiment 3 of the present invention.

[FIG. 9]

FIG. is a plan view of an essential part of the back side showing the state of the back side with the resin sealing body removed in the semiconductor device which employs a BGA structure being Embodiment 4 of the present invention.

[FIG. 10]

FIG. 10 is a cross section of an essential part of the semiconductor device which employs a conventional BGA structure.

[Reference Numerals]

1: BASE SUBSTRATE

1A: ELECTRODE PAD

1B: ELECTRODE PAD

2: SEMICONDUCTOR PELLET

2A: EXTERNAL TERMINAL

3: INSULATING LAYER

4: BUMPER ELECTRODE

5: SLIT

6: BONDING WIRE

7: SEALING BODY

8A, 8B: ELECTRODE PLATE

[Name of Document] ABSTRACT

[Abstract]

[Object] To reduce the size of the semiconductor device and to increase the operating speed of the semiconductor device.

[Solving Means] In a semiconductor device in which a semiconductor pellet 2 is mounted on a pellet mounting area of the main surface of a base substrate 1, and first electrode pads 1B mounted on the rear surface of the base substrate 1 are electrically connected to external terminals 2A arranged on the main surface of the semiconductor pellet 2, the semiconductor pellet 2 is mounted on the pellet mounting area of the main surface of the base substrate 1 with its main surface downward, a second electrode pads 1A electrically connected to the first electrode pads 1B are arranged on the rear surface of the base substrate 1, and the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A of the base substrate 1 are electrically interconnected through bonding wires 6 passing through slits 5 formed in the base substrate 1.

[Selected Figure] FIG. 3

【書類名】　　図面

【図１】

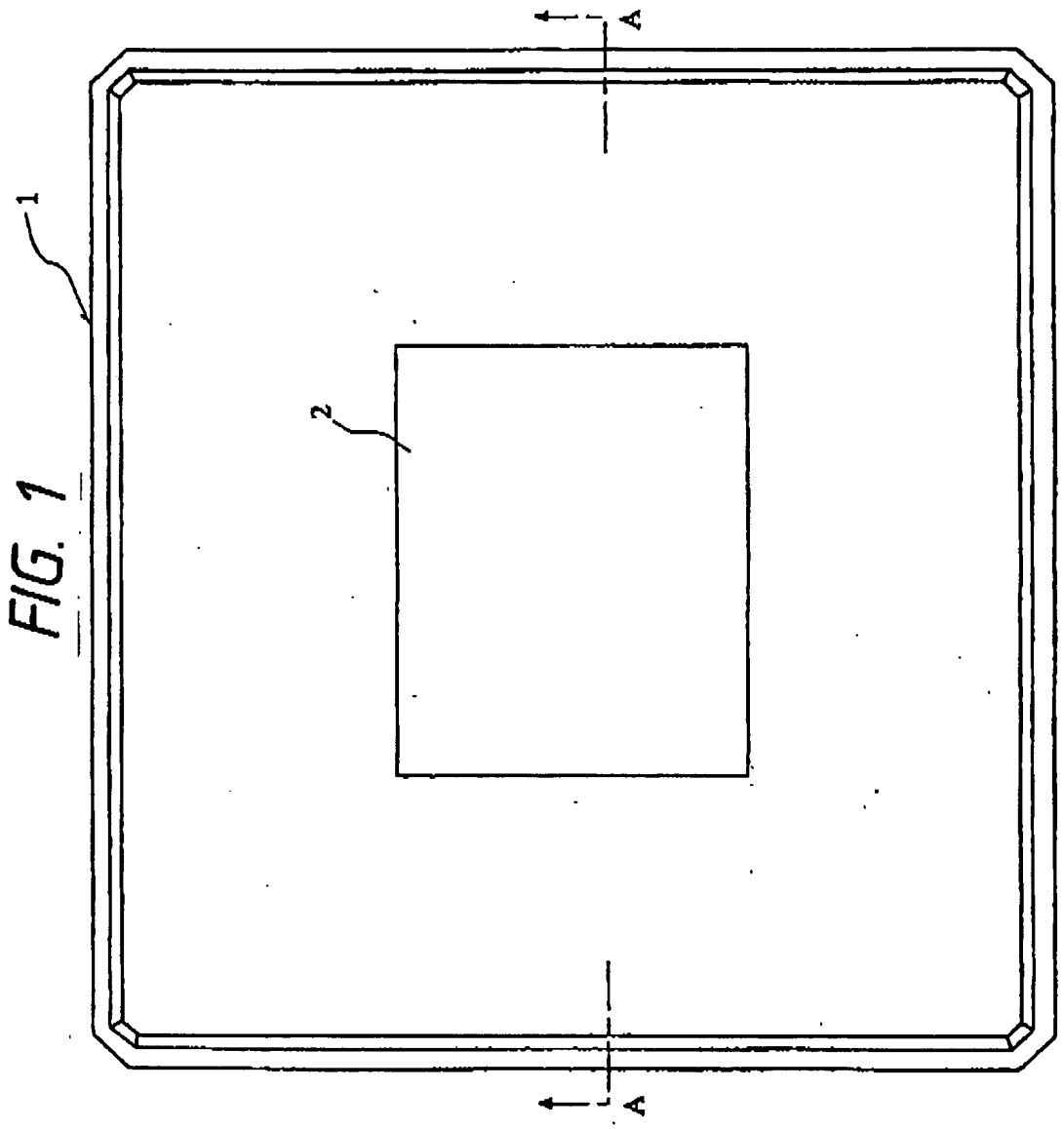
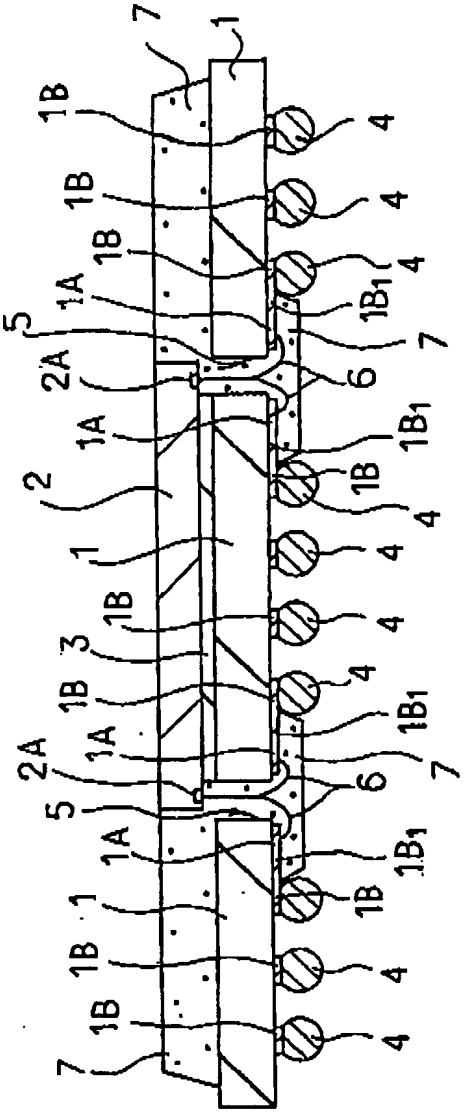


FIG. 1

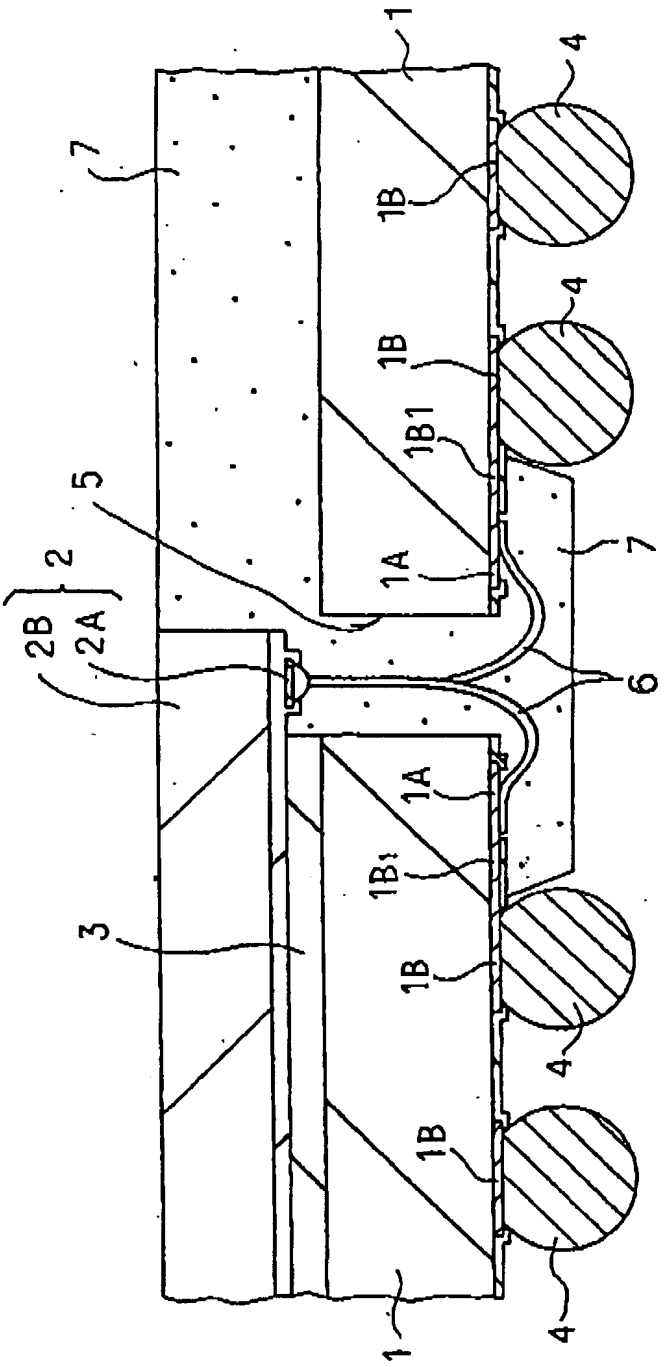
【図２】

FIG. 2



【図３】

FIG. 3



【図４】

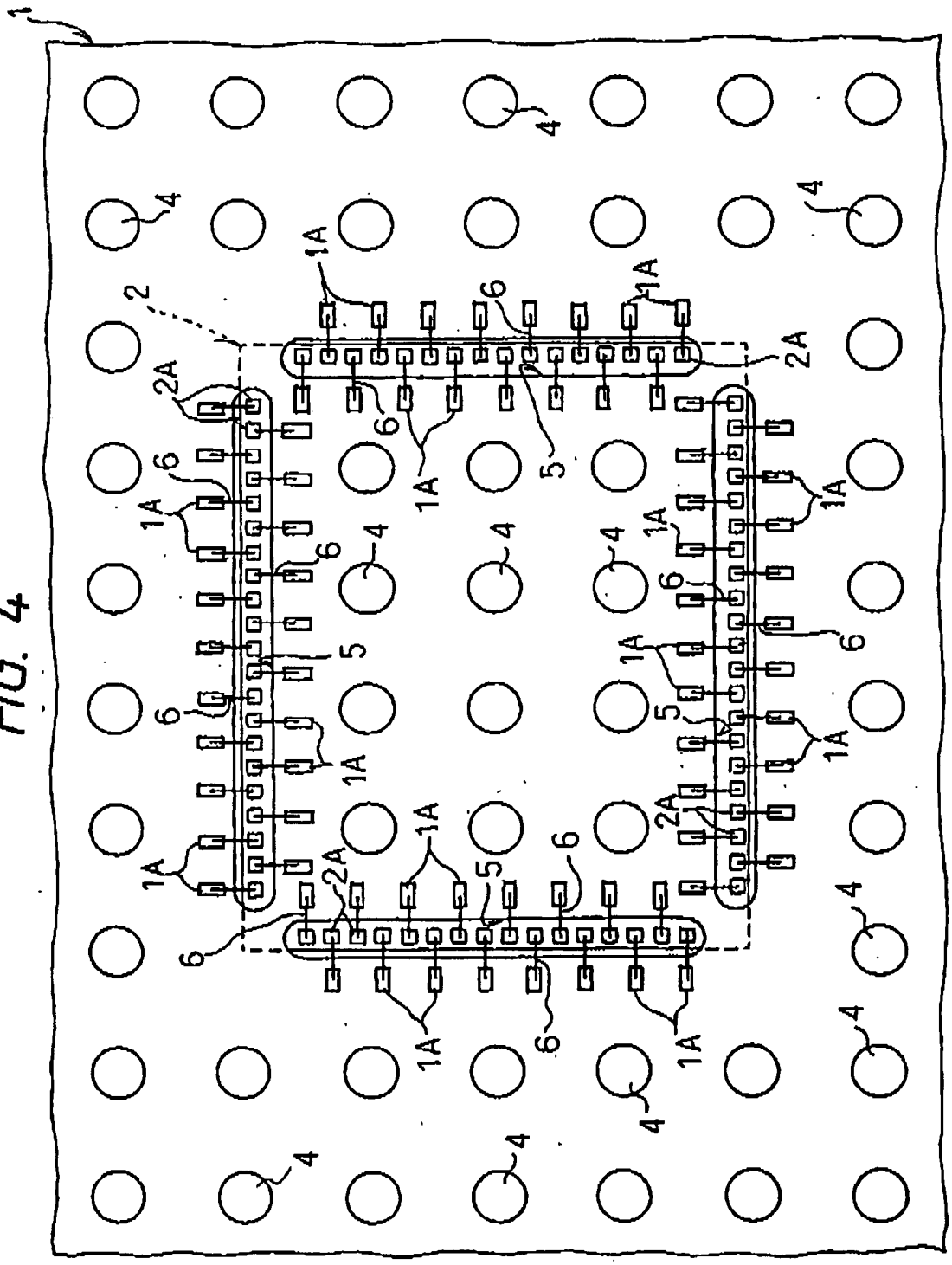
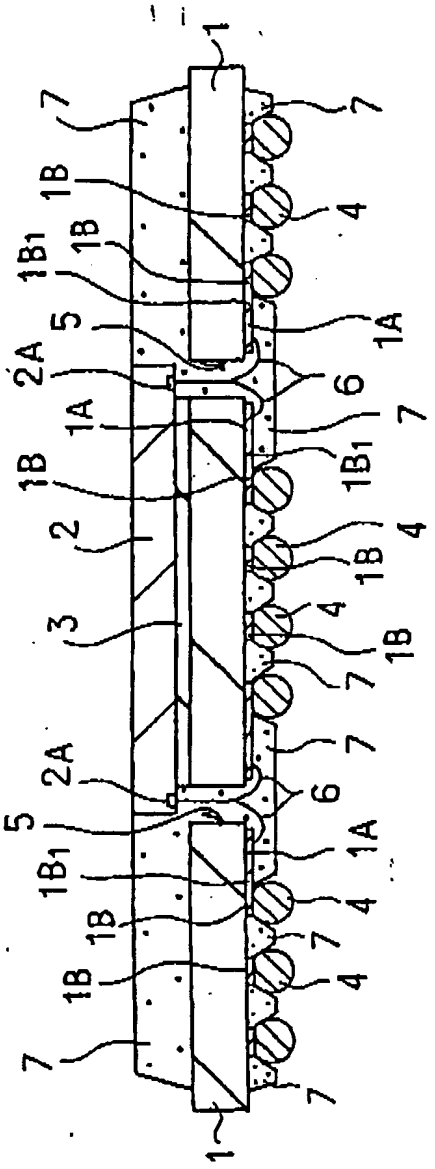


FIG. 4

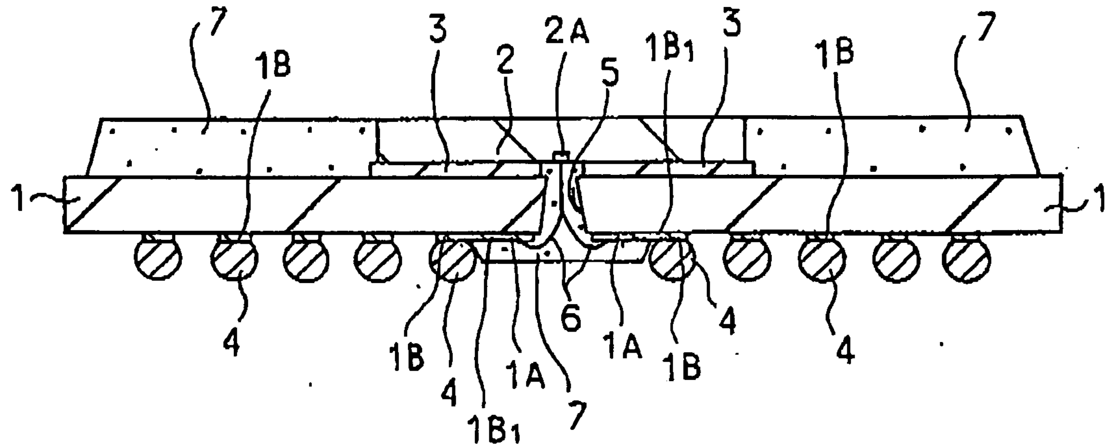
【図５】

FIG. 5



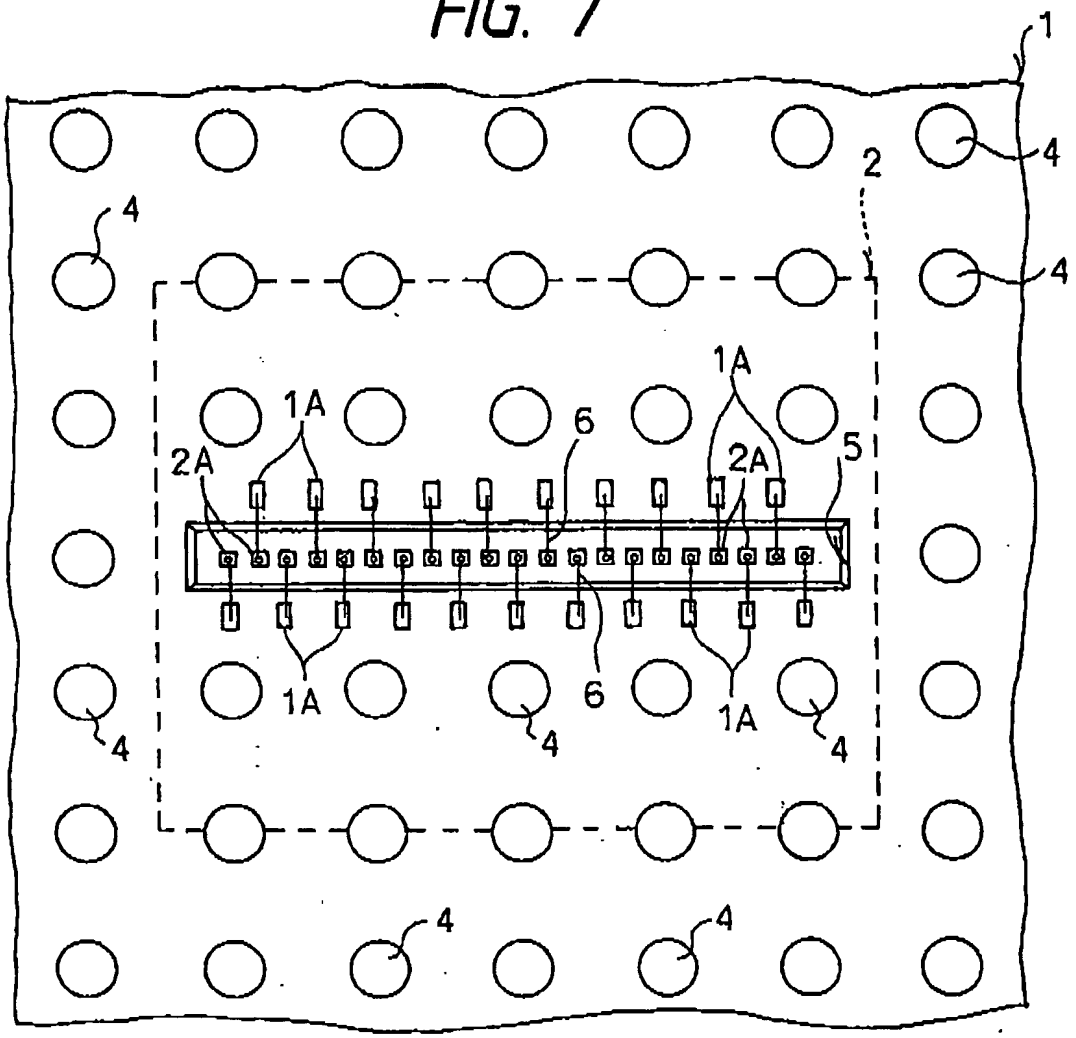
【図６】

FIG. 6



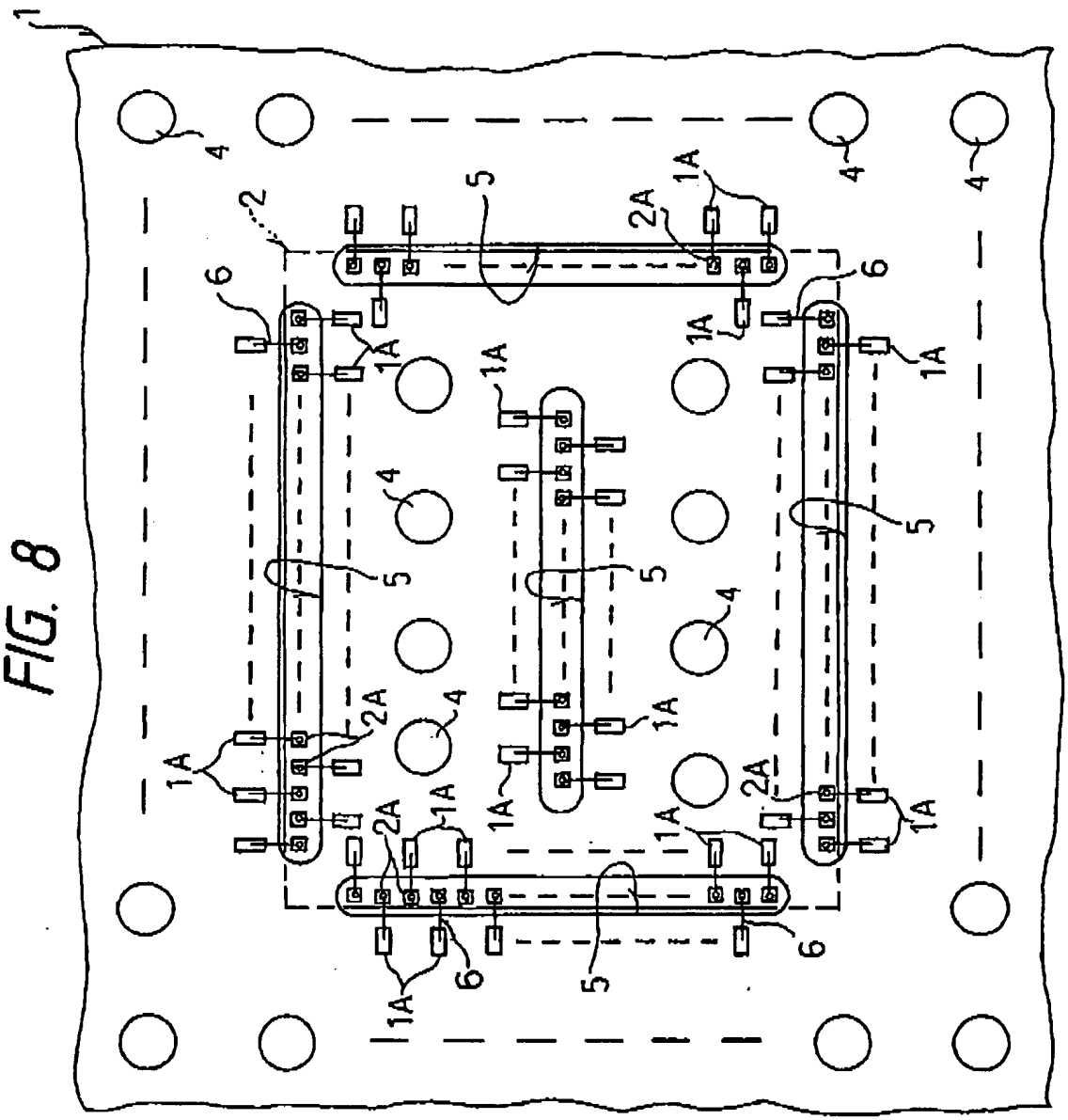
【図７】

FIG. 7



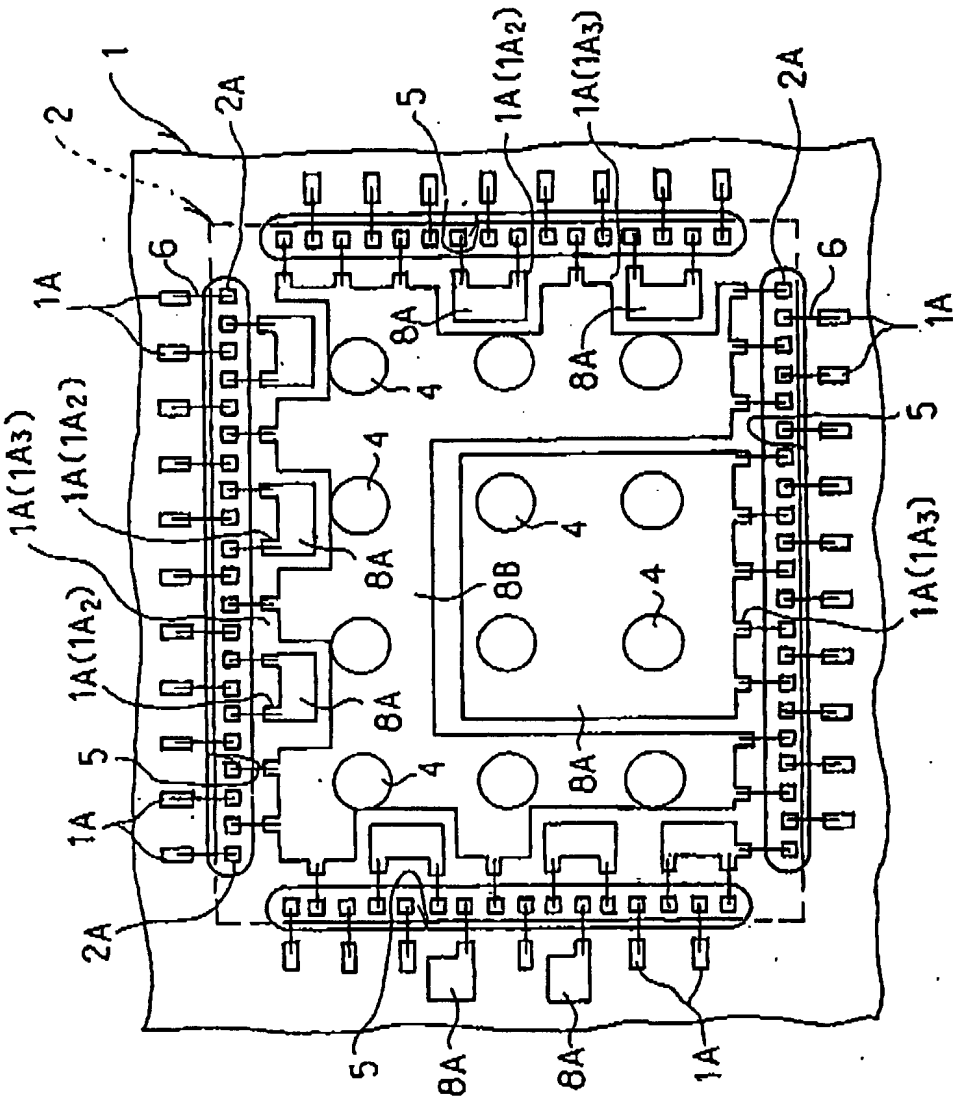
【図８】

FIG. 8



【図９】

FIG. 9


1
2
2A
5
1A(1A2)
1A(1A3)
6
1A
8A
4
8B
2A
5
1A
8A
4
1A(1A3)
1A(1A2)
8A
4
8B
4
1A(1A3)
1A(1A2)
8A
4
8A
5
1A
2A
5
8A
8A
1A

【図１０】

FIG. 10